ANEKANT EDUCATION SOCIETY'S

Tuljaram Chaturchand college of Arts, Science & Commerce, Baramati

Class :- F.Y.B.Sc.[Comp. Sci.]
Department :- Electronic Science
Subject : - Sequential circuit designing
Paper :- II
Subject code :- CSEL1102

QUESTION BANK

Q.1 Answer in short.[1 marks]

1. Define sequential circuit .
2. Define latch .
3. What is flip-flop?
4. Draw symbol of S-R flip-flop.
5. Draw symbol of J-K flip-flop.
6. Draw symbol of T flip-flop.
7. Draw symbol of D flip-flop.
8. Write truth table for positive edge triggered JK flip-flop.
9. Write truth table for positive edge triggered S-R flip-flop.
10. Write truth table for positive edge triggered T flip-flop.
11. Write truth table for positive edge triggered D flip-flop.
12. Define counter .
13. Define Asynchronous counter .
14. Define modules counter
15. Define clock.
16. Write the IC number of Decade counter .
17. Give the types of counter .
18. Define positive edge triggered clock .
19. Define negative edge triggered clock .
20. Define shift register .
21. Write the types of shift register .
22. Define ripple counter .
23. How many flip-flops are required for 3-bit shift register ?
24. How many flip-flops are required for 3-bit Asynchronous counter ?
25. How many flip-flops are required for 3-bit synchronous counter ?
26. What id ring counter ?
27. How we can convert JK flip-flop into T flip-flop.
28. Explain the function of preset and clear terminals in flip-flop.
29. State true or false :
    i. Flip-flop can be used as a memory device .
    ii. Race around condition is overcome in J-K flip-flop.

iii. When J=1, K=1 ,Jk flip-flop is in toggle mode .
iv. A decimal count has a 10 states .
v. Parallel in serial out shift register is used to convert parallel data to serial data .
vi. Riple counters are also called synchronous counter .
vii. Triggered pulse is defined as a pulse that starts a cycle of operation .
viii. Shift register are basically a type of register which has ability to transfer or shift the data .
ix. Counter circuit is usually constructed of a number of flip-flops in cascade.
x. D flip-flop is also known as direct flip-flop.

30. Select the correct alternative :

i. Asynchronous counter differs from synchronous counter
   a) Number of stated in its sequence .
   b) Method of clocking .
   c) Types of flip-flop used .
   d) Value of modulus .

ii. 4-bit binary counter has how many maximum states .
   a) 32
   b) 16
   c) 10
   d) 8

iii. Invalid state of S-R latch occurs when
   a) S = 1 R = 0
   b) S = 0 R = 1
   c) S = 1 R = 1
   d) S = 0 R = 0

iv. If Q = 0 , out put is said to be …….
   a) Set
   b) Reset
   c) Previous state
   d) Current state

v. D flip-flop has…….
   a) One input one output
   b) Two input Two Output
   c) One input Two output
   d) Two input one Output

vi. The number of flip-flop needed Mod-5 counter
   a) 7
   b) 5
   c) 1
   d) 3

vii. A counter is …….
   a) Combinational circuit
   b) Sequential circuit
   c) Both of the above
   d) Non of the above

viii. On MSJK when the master is enable ……
   a) When NOT gate is low
   b) When NOT gate is high
   c) Both the above
   d) Non of the above

ix. How many clock pulses are required to shift a 8-bit data serially…..
   a) 6
   b) 4
   c) 8
   d) 12

Q. Answer in short [2 marks]

31. What is flip-flop? How it stores 1 bit data ?
32. What is difference between Latch and Flip-Flop ?
33. What is race around condition ? How it can be avoided ?
34. Define roll of R-S inputs in R-S flip-flop.
35. State major drawback of R-S flip-flop.
36. A shift register has 4-flip-flop , what is the largest number in binary and decimal?
37. Write excitation table for JK flip-flop.
38. Write excitation table for S-R flip-flop
39. Write excitation table for T flip-flop
40. Write excitation table for D flip-flop
41. Why synchronous counter faster in operation
42. Differentiate synchronous and Asynchronous Counter .
43. Write applications of counter .
44. Write applications of shift register .
45. Write applications of Flip-flop.
46. What is difference between combinational and sequential circuit ?
47. What are the four mode of shift registers and which is the fastest of them ?
48. Write advantages and disadvantages of Flip-flop.
49. What is state diagram ? Draw state diagram for 3-bit down counter .
50. Draw state diagram for 3-bit up- counter .

Q. Long answer questions [4 marks]

1. Explain working of SR flip-flop. Write truth table and logic diagram .
2. Explain working of JK flip-flop. Write truth table and logic diagram .
3. Explain working of T flip-flop. Write truth table and logic diagram .

4. Explain working of D flip-flop. Write truth table and logic diagram .
5. Explain working of MSJK flip-flop. Write truth table and logic diagram .
6. Explain working of 3-bit Asynchronous 3- bit Up counter using T flip-flop.
7. Explain working of 3-bit Asynchronous 3- bit down counter using T flip-flop.
8. Explain working of 3-bit Asynchronous 3- bit Up counter using JK flip-flop.
9. Explain working of 3-bit Asynchronous 3- bit down counter using JK flip-flop.
10. What do you mean by shift register ? Explain any one of shift register .
11. Explain Serial in Serial out shift register .
12. Explain Serial in parallel out shift register .
13. Explain parallel in Serial out shift register .
14. Explain parallel in parallel out shift register .
15. What is modulus counter ? Explain mode -5 .
16. What is modulus counter ? Explain mode -4.
17. What is modulus counter ? Explain mode -6 .
18. Explain Mod -2 and Mod 3 counter .

Q. Long answer questions [6marks]

19. Draw logic diagram of shift register as ring counter . Explain its action in detailed .
20. What do you mean by Modulus of counter ? Construct Mod-7 counter using logic diagram , timing diagram and count sequence .
21. Draw and explain MSJK flip-flop with its truth table and logic diagram .
22. Design 3-bit synchronous up counter using JK flip-flop with K-map . draw its timing diagram .
23. Design 3-bit synchronous down counter using JK flip-flop with K-map . Draw its timing diagram .
24. For a 4-bit SISO shift register draw a timing diagram to show shifting of data 0111 into it.Assume that register initially contain all 0000 data.
25. Draw the circuit diagram of up/down counter . Explain its action with stake table and timing diagram .
26. How will you get T flip-flop from JK flip flop and draw logic diagram and truth table of each
27. How will you get D flip-flop from S-R flip flop and draw logic diagram and truth table of each .

Q. Long answer questions [12marks]

1. Design 4-bit synchronous up counter using JK flip-flop.
2. Design 4-bit synchronous down counter using JK flip-flop.
3. Design 4-bit synchronous up counter using T flip-flop.
4. Design 4-bit synchronous Down counter using T flip-flop.
5. Explain 4-bit ring counter right shift register.
6. Explain universal 4-bit shift register .
7. What do you mean by race around condition in connection with JK flip-flop ? Draw MSJK flip-flop system and explain it oppression showing that it eliminate race around condition .