FIELD EFFECT TRANSISTOR (FET)

Basic Ideas

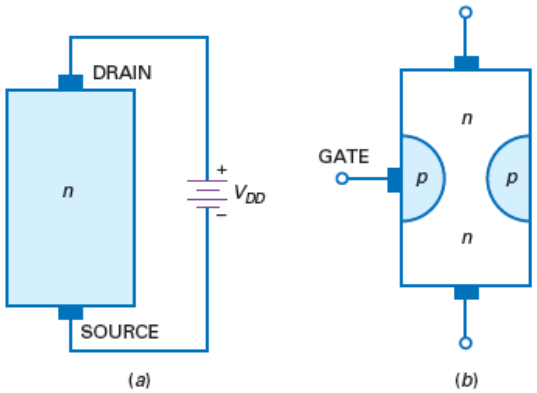

Figure 1 (*a*) Part of JFET; (*b*) single-gate JFET.

Figure 1 (a) shows a piece of *n*-type semiconductor. The lower end is called the **source,** and the upper end is called the **drain.** The supply voltage *VDD* forces free electrons to flow from the source to the drain. To produce a JFET, a manufacturer diffuses two areas of *p*-type semiconductor into the *n*-type semiconductor, as shown in Fig. 1 (b) These *p* regions are connected internally to get a single external **gate** lead.

Field Effect

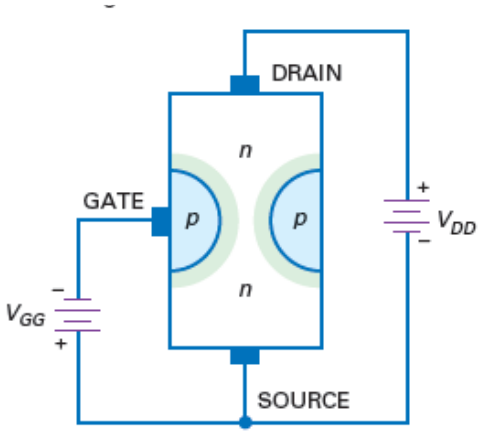

Figure 2: Normal biasing of JFET.

Figure 2 shows the normal biasing voltages for a JFET. The drain supply voltage is positive, and the gate supply voltage is negative. The term **field effect** is

related to the depletion layers around each *p* region. These depletion layers exist because free electrons diffuse from the *n* regions into the *p* regions. The recombination of free electrons and holes creates the depletion layers.

Reverse Bias of Gate

In Fig. 2, the *p*-type gate and the *n*-type source form the gate-source diode. With a JFET, we always *reverse-bias* the gate-source diode. Because of reverse bias, the gate current I_G is approximately zero, which is equivalent to saying that the JFET has an almost infinite input resistance.

A typical JFET has an input resistance in the hundreds of megohms. This is the big advantage that a JFET has over a bipolar transistor. It is the reason that JFETs excel in applications in which a high input impedance is required. One of the most important applications of the JFET is the *source follower,* a circuit like the emitter follower, except that the input impedance is in the hundreds of megohms for lower frequencies.

Gate Voltage Controls Drain Current

In Fig. 2, electrons flowing from the source to the drain must pass through the narrow **channel** between the depletion layers. When the gate voltage becomes more negative, the depletion layers expand and the conducting channel becomes narrower. The more negative the gate voltage, the smaller the current between the source and the drain.

The JFET is a **voltage-controlled device** because an input voltage controls an output current. In a JFET, the gate-to-source voltage V_{GS} determines how much current flows between the source and the drain. When V_{GS} is zero, maximum drain current flows through the JFET. This is why a JFET is referred to as a normally on device. On the other hand, if V_{GS} is negative enough, the depletion layers touch and the drain current is cut off.

Schematic Symbol

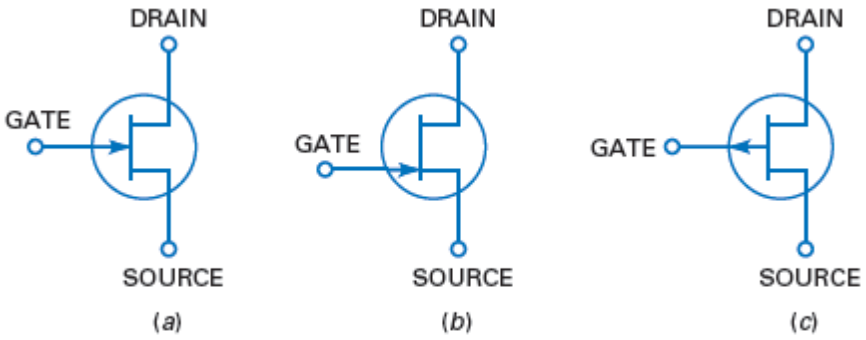

Figure 3: (*a*) Schematic symbol; (*b*) off set-gate symbol; (*c*) *p*-channel symbol

The JFET of Fig. 2 is an *n-channel JFET* because the channel between the source and the drain is an *n*-type semiconductor. Figure 3 (a) shows the schematic symbol

for an *n*-channel JFET. In Figure 3(b) shows an alternative symbol for an *n*-channel JFET. There is also a *p*-channel JFET. The schematic symbol for a *p*-channel JFET, shown in Fig. 3(c), is similar to that for the *n*-channel JFET, except that the gate arrow points in the opposite direction. The action of a *p*-channel JFET is complementary; that is, all voltages and currents are reversed. To reverse-bias a *p*-channel JFET, the gate is made positive in respect to the source. Therefore, V_{GS} is made positive.

Drain Curves

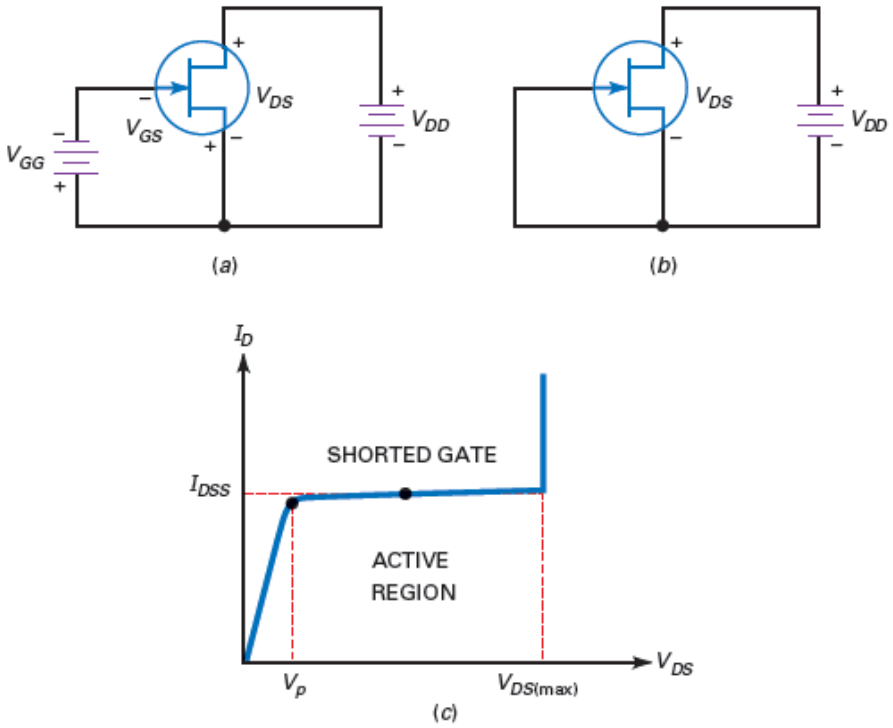

Figure 4 : (*a*) Normal bias; (*b*) zero gate voltage; (*c*) shorted gate drain current.

Figure 4(a) shows a JFET with normal biasing voltages. In this circuit, the gate-source voltage V_{GS} equals the gate supply voltage V_{GG}, and the drain-source voltage V_{DS} equals the drain supply voltage V_{DD}.

Maximum Drain Current

If we short the gate to the source, as shown in Fig. 4(b), we will get maximum drain current because $V_{GS} = 0$. Figure 4 (c) shows the graph of drain current I_D versus drain-source voltage V_{DS} for this shorted-gate condition. The drain current increases rapidly and then becomes almost horizontal when V_{DS} is greater than V_P.

The drain current becomes almost constant because when V_{DS} increases, the depletion layers expand. When $V_{DS} = V_P$, the depletion layers are almost touching. The narrow conducting channel therefore pinches off or prevents a further increase in current. This is why the current has an upper limit of I_{DSS}.

The active region of a JFET is between V_P and $V_{DS\,(max)}$. The minimum voltage V_P is called the **pinch off voltage,** and the maximum voltage $V_{DS\,(max)}$ is the *breakdown voltage.* Between pinch off and breakdown, the JFET acts like a current source of approximately I_{DSS} when $V_{GS} = 0$. I_{DSS} stands for the current drain to source with a shorted gate. This is the maximum drain current a JFET can produce.

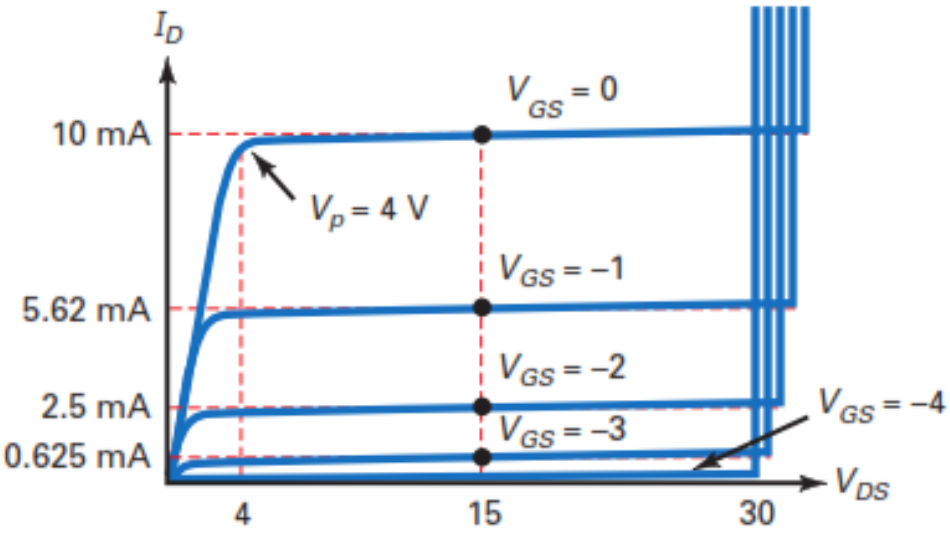

Figure 5: Drain curves

The Ohmic Region

In Fig. -5, the pinch off voltage separates two major operating regions of the JFET. The almost-horizontal region is the **active region**. The almost-vertical part of the drain curve below pinch off is called the **ohmic region.** When operated in the ohmic region, a JFET is equivalent to a resistor with a value of approximately:

$$R_{DS} = \frac{V_P}{I_{DSS}}$$

R_{DS} is called the *ohmic resistance of the JFET.* In Fig. 5, $V_P = 4$ V and $ID_{SS} = 10$ mA. Therefore, the ohmic resistance is

$$R_{DS} = \frac{4\text{ V}}{10\text{ mA}} = 400\ \Omega$$

If the JFET is operating anywhere in the ohmic region, it has an ohmic resistance of 400 Ohm .

Gate Cutoff Voltage

Figure 5 shows the drain curves for a JFET with an I_{DSS} of 10 mA. The top curve is always for V_{GS} = 0, the shorted-gate condition. In this example, the pinch off voltage is 4 V and the breakdown voltage is 30 V. The next curve down is for V_{GS} = -1 V, the next for V_{GS}=-2 V, and so on. As you can see, the more negative the gate-source voltage, the smaller the drain current.

The bottom curve is important. Notice that a V_{GS} of -4 V reduces the drain current to almost zero. This voltage is called the **gate-source cutoff voltage** and is symbolized by $V_{GS(off)}$ on data sheets. At this cutoff voltage, the depletion layers touch. In effect, the conducting channel disappears. This is why the drain current is approximately zero.

In Fig. 5, notice that

$$V_{GS(off)} = -4 \text{ V and } V_P = -4 \text{ V}$$

This is not a coincidence. The two voltages always have the same magnitude because they are the values where the depletion layers touch or almost touch.

Therefore:

$$\mathbf{V_{GS(off)} = -V_P}$$

The Transconductance Curve

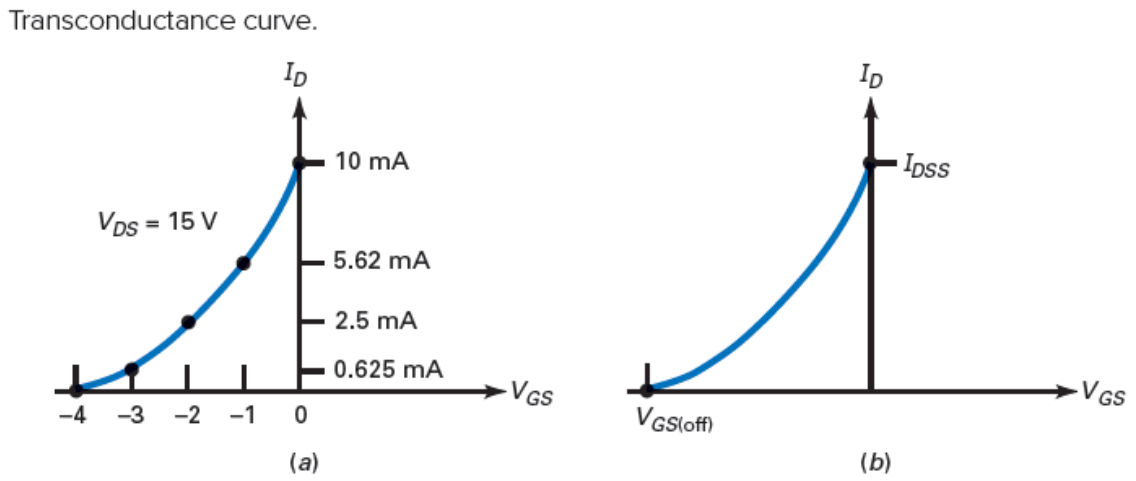

Figure 6: The transconductance curve of a JFET

The **transconductance curve** of a JFET is a graph of I_D versus V_{GS}. By reading the values of *ID* and *VGS* of each drain curve in Fig. 5, we can plot the curve of Fig. 6*a*. Notice that the curve is nonlinear because the current increases faster when V_{GS} approaches zero.

Any JFET has a transconductance curve like Fig. 6*b*. The end points on the curve are $V_{GS(off)}$ and I_{DSS}. The equation for this graph is:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

Because of the squared quantity in this equation, JFETs are often called *square-law devices.*

Applications of JFET

1] The JFET Analog Switch

JFET is used for *analog switching.* In this application, the JFET acts as a switch that either transmits or blocks a small ac signal. To get this type of action, the gate-source voltage V_{GS} has only two values: either zero or a value that is greater than $V_{GS(off)}$. In this way, the JFET operates either in the ohmic region or in the cutoff region.

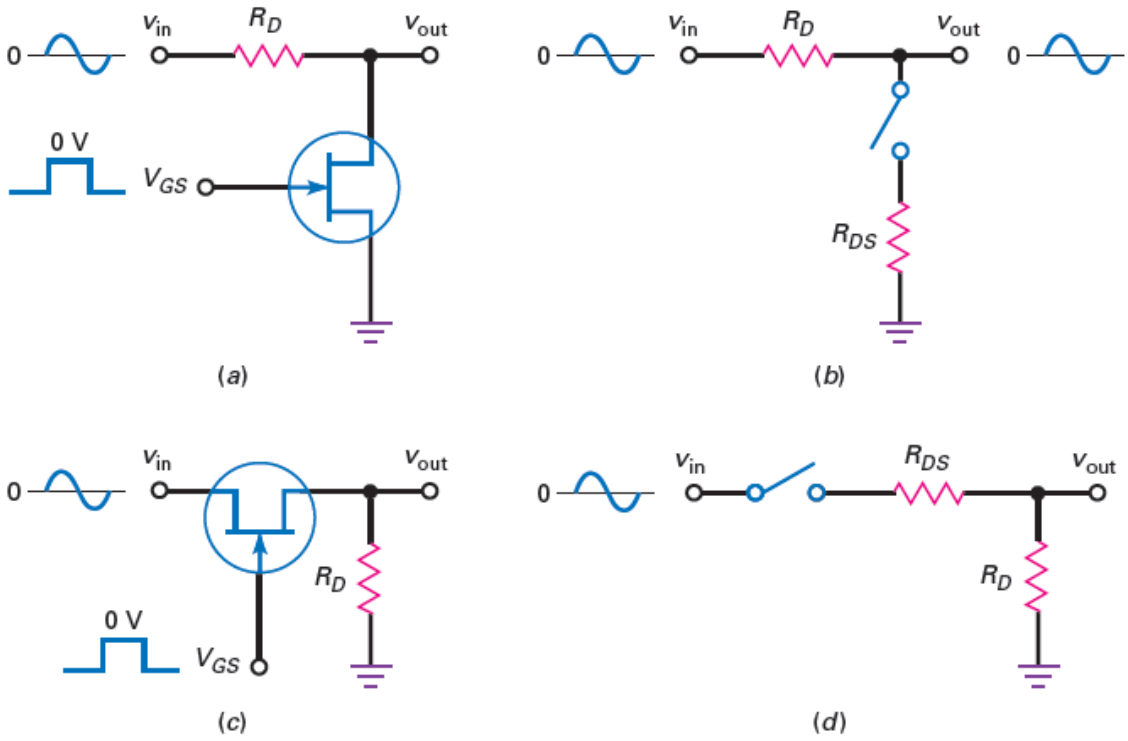

Figure 7: JFET analog switches: (a) Shunt type; (b) shunt-equivalent circuit; (c) series type; (d) series-equivalent circuit.

Shunt Switch:

Figure 7(*a*) shows a JFET **shunt switch.** The JFET is either conducting or cutoff, depending on whether V_{GS} is high or low. When V_{GS} is high (0 V), the JFET operates in the ohmic region. When V_{GS} is low, the JFET is cut off. Because of this, we can use Fig. 7(*b*) as an equivalent circuit.

When V_{GS} is high, the JFET operates in the ohmic region and the switch of Fig. 7(*b*) is closed and V_{out}= 0. When V_{GS} is low, the JFET cuts off and the switch of Fig. 7(*b*) opens and $V_{out}=V_{in}$ Therefore, the JFET shunt switch either transmits the ac signal or blocks it.

Series Switch:

Figure 7(*c*) shows a JFET **series switch,** and Fig. 7(*d*) is its equivalent circuit. When V_{GS} is high, the switch is closed. In this case, the output approximately equals the input. When V_{GS} is low, the JFET is open and is approximately zero.

2] The JFET as an Analog Multiplexer

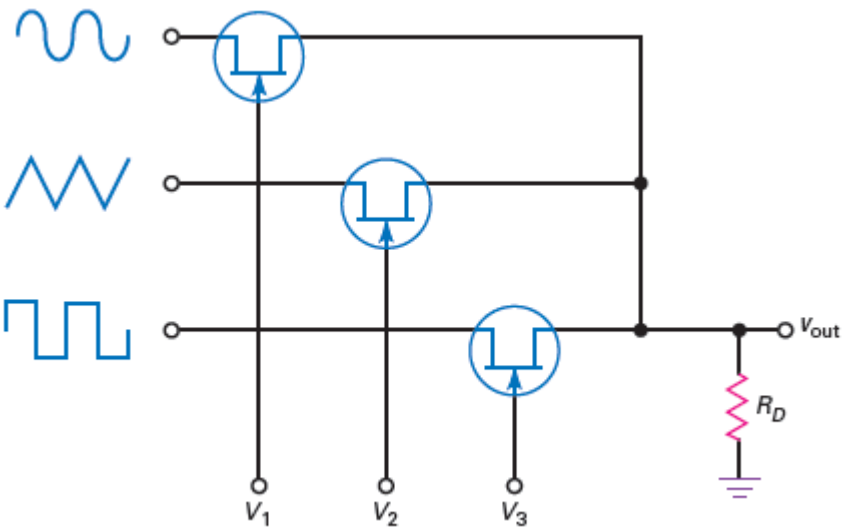

Figure 8: JFET as an analog Multiplexer

Multiplex means "many into one." Figure 8 shows an *analog multiplexer,* a circuit that steers one or more of the input signals to the output line. Each JFET acts like a series switch. The control signals (V_1, V_2, and V_3) turn the JFETs on and off. When a control signal is high, its input signal is transmitted to the output. For instance, if V_1 is high and the others are low, the output is a sine wave. If V_2 is high and the others are low, the output is a triangular wave. When V_3 is the high input, the output is a square wave. Normally, only one of the control signals is high; this ensures that only one of the input signals is transmitted to the output.

3] The JFET as Variable resistor [Voltage-Controlled Resistance]

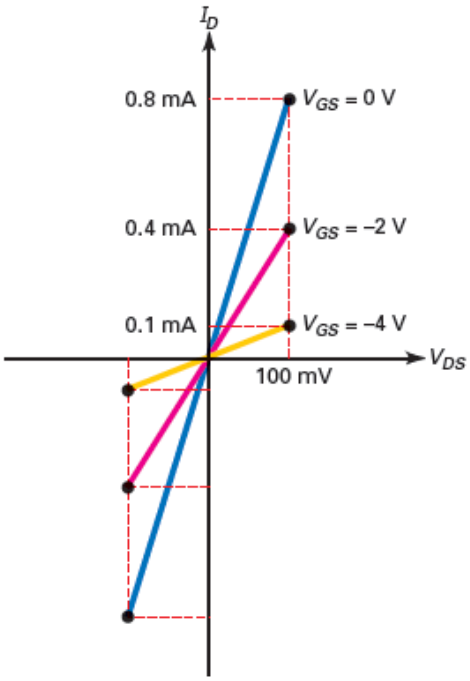

Figure 9: JFET as Voltage controlled resistor

When a JFET operates in the ohmic region, it usually has V_{GS} = 0 to ensure hard saturation. But there is an exception. It is possible to operate a JFET in the ohmic region with V_{GS} values between 0 and $V_{GS(off)}$. In this case, the JFET can act like a *voltage-controlled resistance.*

Figure 9 shows the drain curves of a 2N5951 JFET near the origin with V_{DS} less than 100 mV. In this region, the small-signal resistance *rds* is defined as the drain voltage divided by the drain current:

$$r_{ds} = \frac{V_{DS}}{I_D}$$

In Fig. 9 It is seen that r_{ds} depends on which V_{GS} curve is used. For V_{GS} = 0, r_{ds} is minimum and equals R_{DS}. As V_{GS} becomes more negative, r_{ds} increases and becomes greater than R_{DS}.

For instance, when V_{GS} = 0 in Fig.9, we can calculate:

$$r_{ds} = \frac{100\text{ mV}}{0.8\text{ mA}} = 125\ \Omega$$

When $V_{GS} = -2$ V:

$$r_{ds} = \frac{100\text{ mV}}{0.4\text{ mA}} = 250\ \Omega$$

When $V_{GS} = -4$ V:

$$r_{ds} = \frac{100\text{ mV}}{0.1\text{ mA}} = 1\text{ k}\Omega$$

This means that a JFET acts like a voltage-controlled resistance in the ohmic region.

UNIVERSITY QUESTIONS

1) Draw symbol of P-channel JFET [1]
2) Draw symbol of N-channel JFET [1]
3) Discuss the construction and working of N-channel JFET. Draw its characterstics curves. [5]
4) A JFET has Vp= 5V and I_{DSS}=100mA.What is its ohmic resistance?[1]
   Ans: The ohmic resistance is given by

$$R_{DS} = \frac{V_P}{I_{DSS}}$$

$$=5V/100mA$$
$$= 50\Omega$$

5) When V_{GS} of JEFT changes from 2.2V to 2.1V,the drain current raises from 1.1mA to 1.4mA. Find the value of transconductance. [1]
   Ans: Conductance of FET=Reciprocal of resistance =$\Delta Id/\Delta V_{GS}$

$$=\frac{1.4-1.1mA}{2.2-2.1V}$$

$$=\frac{0.3}{0.1} \text{ X } 10^{-3}$$

$$= 3 \text{ x } 10^{-3} \text{ mho}$$

6) When a reverse gate voltage of 20V is applied to a FET, the gate current is $10^{-3}\mu A$.Find the resistance between the gate and source.[1]
   Ans: Use Ohm's law

Resistance between the gate and source $[R_{in}\}=\frac{\text{Reverse gate voltage}}{\text{Gate current}}$

$$=20V/10^{-3}\mu A$$

$$=20 \text{ x } 10^{-9}\ \Omega$$
